ABSTRACT OF THE DISCLOSURE

A processing method, a chip set and a controller for supporting message signaled interrupt. A memory write transaction on a PCI bus is monitored. When the address of the system memory specified in the interrupt message of the write transaction is located at a range of a reserved interrupt address, the interrupting service sequence is performed. The reserved interrupt address is located in an address of a system memory. Thus, the data to be processed and the system-specified message are written in the buffer and arranged in sequence. The problem of "write buffer latency" is resolved, and is irrelevant to the level of the PCI bus. Many system specified messages can be stored in the system memory, so that multiple system message signaled interrupts issue from different peripheral components can be processed in the same interrupt service routine.